AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 12, with the following rewritten paragraph:

Generally, a hold type image display apparatus such as an LCD apparatus or an EL display apparatus is constructed by a plurality of data lines (or signal lines) driven by a data line driver circuit, a plurality of gate lines (or scan lines) driven by a gate line driver circuit, and pixels each located at one intersection between the data lines and the gate lines. In such a hold type image display apparatus, the quality of display deteriorates due to the residual image phenomenon caused by the low response speed and the hold operation. This will be explained later in detail.

Please replace the paragraph beginning at page 9, line 30, with the following rewritten paragraph:

In Fig. 4, which illustrates a detailed circuit diagram of the gate line driver circuit 13 of Fig. 1, the gate line driver circuit 13 is constructed by a shift register circuit 131 for shifting a vertical start pulse signal VST as shown in Fig. 5 in synchronization with a vertical clock signal VCK as shown in Fig. 5, and an output buffer circuit 132 formed by amplifiers (usually, voltage-follower-type operational amplifiers) 1321, 1322, 1323, 1324, ..., 132n-1, 132n. Note that one vertical start pulse signal [[VSP]] VST is generated per one frame period. This shift register circuit 131 is formed by serially-connected D-type flip-flops 1311, 1312, 1313, 1314, ..., 131n-1, 131n clocked by rising edges of the vertical clock signal VCK to generate gate line signals (or scan line signals) as shown in Fig. 5 on the gate lines GL_1, GL_2, GL_3, GL_4, ..., GL_{n-1}, GL_n, respectively.

Please replace the paragraph beginning at page 19, line 21, with the following rewritten paragraph:

In Fig. 19, which illustrates a detailed circuit diagram of the gate line driver circuit 2 of Fig. 16, the gate line driver circuit 3 is constructed by shift register circuits 31 and 32 for shifting a vertical start pulse signal VST as shown in Fig. 20 in synchronization with a vertical clock signal VCK as shown in Fig. 20, a gate circuit 33 and an output buffer circuit 34 formed by

amplifiers 341, 342, 343, 344, ..., 34n-1, 34n. Note that two vertical start pulse signals [[VSP]] VST are generated per one frame period.

Please replace the paragraph beginning at page 24, line 15, with the following rewritten paragraph:

The data register circuit 22' latches an 8-bit ~~gradating~~ gradation video data signal VD represented by B_0, B_1, ..., B_7 in accordance with the latch signals LA1, LA2, ..., LA(m/2-1), LAm/2. The data register circuit 22' has the same configuration as the data register circuit 22 of Fig. 17. That is, the data register circuit 22' is formed by 8 D-type flip-flops 221 clocked by the latch signal LA1 to latch digital video data D1 or D3 of the gradation video signal VD as shown in Fig. 25, 8 D-type flip-flops 222 clocked by the latch signal LA2 to latch digital video data D3 or D4 of the gradation video signal VD as shown in Fig. 25, ..., 8 D-type flip-flops 22 (m/2-1) clocked by the latch signal LA(m/2-1) to latch digital video data Dm-3 or Dm-2 of the gradation video signal VD as shown in Fig. 25, and 8 D-type flip-flops 22 clocked by the latch signal LAm/2 to latch digital video data Dm-2 or Dm of the gradation video signal VD as shown in Fig. 25. In this case, the digital video data D1, D2, D5, ..., Dm-3, Dm-2, D3, D4, D7, ..., Dm-1, Dm of the 8 bit gradation video signal VD are sequentially generated from a signal processing circuit (not shown). In more detail, in a first horizontal period, the digital video data D1, D2, D5, ..., Dm-3, Dm-2, D3, D4, D7, ..., Dm-1, Dm are sequentially generated, and in a second horizontal period, alternately with the first horizontal period, the digital video data D3, D4,D7, ..., Dm-1, Dm, D1, D2, D5, ..., Dm-3, Dm-2 are sequentially generated.